REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1-6 remain active in this case, Claim1 having been amended and Claim 7 canceled by the present amendment, and Claims 8-25 having been withdrawn from consideration as directed to a non-elected invention.

In the outstanding Office Action, the specification was objected to as including an informality requiring correction; Claim 1 was objected to as including language requiring clarification; and Claims 1-7 were rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Mizuno et al., (Publication No. US2003/0102904A1, hereinafter called "Mizuno").

First, the informalities identified in the speciation and Claim 1 have been corrected herewith. No new matter has been added.

In light of the outstanding ground for rejection, Claim 1 has been amended to include the feature stated in original Claim 7 and Claim 7 has been canceled. No new matter has been added.

Briefly recapitulating, amended Claim 1 is directed to a semiconductor integrated circuit in which signals propagate between circuit blocks belonging to different respective power domains, and in which an ESD (electrostatic discharge) protection network is formed. The claimed invention thereby includes a countermeasure against the case where a circuit in a chip cannot be protected in spite of the attempt to protect the chip using the ESD protection network. The present invention uses an element having a high input withstanding voltage (for example, as stated in Claim 4 a MOS transistor having a relatively thick gate oxide) to prevent the element from being broken when an ESD causes voltage input from a signal line

of an interface to exceed the breakdown voltage of the element even in the case where the parasitic resistance of a power supply wire extending to the ESD protection network and/or the equivalent parasitic resistance of the ESD protection network is high.

By virtue of the claimed invention, an ESD immunity level can be increased without expanding the power supply wire or increasing the size of a protection element. Consequently, special manufacturing processes, increases in chip area, and/or increases in chip cost are unnecessary to increase the ESD immunity level in comparison with conventional ESD protection measures. Also, the same ESD immunity level as that of the prior art can be achieved with a smaller chip area and at a lower cost. Thus, it is believed to be clear that the claimed invention does not merely aim at applying a high voltage as an operating voltage, although that may be a subsidiary benefit.

The semiconductor integrated circuit device of Mizuno is cited as a semiconductor integrated circuit device with excellent high speed and low power operation characteristics, and the outstanding Official Action relies on Mizuno as teaching "that the signal input element has an input withstanding voltage which is higher than that of other elements of the circuit block as disclosed in Col. 15, lines 26-30."[1].

However, as taught by Mizuno, a MOS transistor having a thick gate oxide film is inserted between a power supply and a circuit as a switch to reduce an off leak current a tunneling current of a gate. With this structure, a high voltage can be applied as an operating voltage to reduce ON resistance of the MOS transistor in Mizuno. Therefore, Mizuno basically differs from the present invention in structure, and Mizuno does not disclose or suggest structure of a semiconductor integrated circuit in which an ESD protection network is formed in signal lines between circuit blocks employing different power supply voltages.

[1] Office Action, page 4, second full paragraph.

Generally, an element having a thick gate oxide (film) reduces an operating speed. Therefore, even if the prior art discloses a structure of a semiconductor integrated circuit in which an ESD protection network is formed, absent proscribed hindsight, a person skilled in the art would not be led to use an element which reduces operating speed, as disclosed in Mizuno, in a circuit to which a signal line voltage is input, by simply combining the admitted prior art and Mizuno. Accordingly, it is respectfully submitted that the outstanding ground for rejection is overcome by the present amendment and that Claims 1-6 patentably define over the applied prior art.

Consequently, in view of the present amendment and in light of the above comments, no further issues are believed be outstanding, and the present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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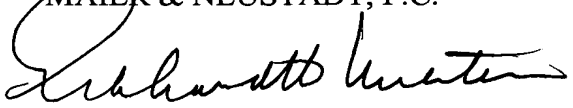

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